Printed Pages: 6 **CA405/NMCAE-014**

(Following Paper ID and Roll No. to be filled in your Answer Books)	
Paper ID : 214405	**Roll No.**

M.C.A.

Theory Examination (Semester-IV) 2015-16

ADVANCE COMPUTER ARCHITECTURE

Time : 3 Hours ***Max. Marks : 100***

Section-A

Note: Attempt all the parts. All parts carry equal marks. Write answer of each part in short. (10×2 = 20)

1. (a) Define state and cycle.

(b) What are the performance differences between write update and write invalidate protocols?

(c) What is Reliability, Availability and Dependability with reference to storage systems?

(d) Is n-cycle pipelining increases speed by n time? Justify your answer.

(e) What are centralized shared memory architectures and symmetric shared memory multiprocessors?

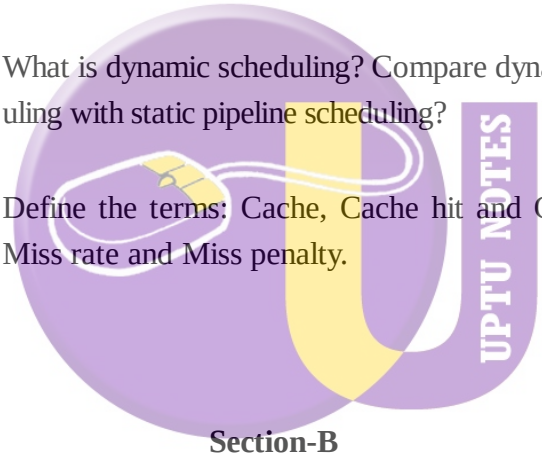
(f) What are the merits of MIMD multiprocessors?

(g) Larger block sizes will reduce compulsory misses. Is the statement true or false? Justify you answer.

(h) How data hazards can be minimized?

(i) What is dynamic scheduling? Compare dynamic scheduling with static pipeline scheduling?

(j) Define the terms: Cache, Cache hit and Cache miss. Miss rate and Miss penalty.



Section-B

2. Attempt any five questions from this section. (5×10 = 50)

(a) Describe set-associative mapping scheme for cache memory.

(b) Describe expression for performance, throughput, sopt and total instructions execution time for pipelining processing.

(c) Discuss in detail various Interconnect architectures for MIMD computers.

(d) What is Cache Coherence Problem? What is a snooping cache? Discuss with example the Write Through and Write Once protocols for Cache consistency.

(e) What is multithreading and explain in detail about the types of multithreading.

(f) Define parallel computing? What are the fundamental issues in parallel processing? Why parallel computing is required?

(g) Write short notes on:

i. Condition compilation

ii. Master and synchronization constructions.

(h) Explain in detail about the various hit time reduction techniques.

Section-C

Note : Attempt any two questions from this section.

(2×15 = 30)

3. Analyse the data dependencies among the following statements:

S1: Load R1, 1024 /R1←1024/

S2: Load R2, M(10) /R2←Memory(10)/

S3: Add R1, R2 /R1←(R1) + (R2)/

S4: Store M (1024), R1 /Memory (1024) ← (R1)/

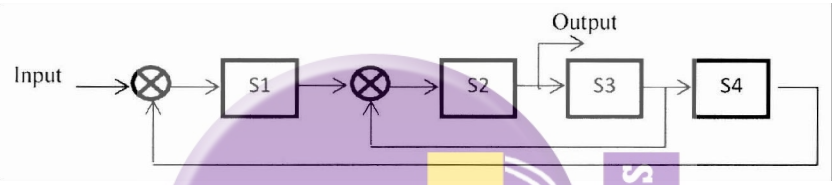
S4: Store M (R2), 1024 /Memory (64) ← 1024/

Note that (*Ri*) means that the content of register *Ri* and *Memory (10)* contains 64 initially.

i. Draw a dependence graph to show all the dependencies.

ii. Are there any resource dependencies if only one copy of each functional unitis available in the CPU?

4. Consider the following pipelined processor with four stages. This pipeline has a total evaluation time of six clock cycles. All successor stages must be used after each clock cycle.



i. Specify the reservation table for this pipeline with six columns and four rows?

ii. List the set of forbidden latencies between task initiations.

iii. Draw the state diagram which shows all possible latency cycles.

iv. List all greedy cycles from the state diagram.

v. Determine the minimal average latency (MAL).

5. Explain how instruction set compiler technology CPU implementation & control and memory hierarchy effect the CPU performance. Justify the effects in terms of program length, clock rate and effective CPI.