Printed Pages : **NEC024**

(Following Paper ID and Roll No. to be filled in your Answer Books)

PAPER ID : **Roll No.** | | | | | | | | | | |

B.TECH

Theory Examination (Semester-VI) 2015-16

ADVANCED DIGITAL DESIGN AND VERILOG

Time : 3 Hours ***Max. Marks : 100***

SECTION-A

1. Attempt all parts. All parts carry **equal** marks. Write answer of each part in short**. (2 x 10 =20)**

a) What is the purpose of the **`timescale** compiler directive?

b) Implement a full adder using a 3 to 8 decoder.

c) Draw the logic diagram of clocked D flip-flop.

d) How long will it take to shift the hexadecimal number 'AB' into the 54/74164 (SIPO) if 5MHz clock is used?

e) Mention any two differences between Synchronous and Asynchronous counter.

f) Compare Moore and Mealy model of synchronous sequential circuit.

g) What are tristate gates?

h) Define Path Delay?

i) Mention data types used in Verilog HDL.

j) How to Eliminate Hazards in a digital circuits?

SECTION-B

2. Attempt any **five** questions from this section. **(10 x 5 = 50)**

(a) Determine whether the function f (x1, x2, x3, x4) = Σ (0, 1, 3, 4, 5, 6, 7, 12, 13) is a threshold function, and if it is, find a weight-threshold vector.

(b) Given a logic design and implementation using the multiplexers for F1= Σ m(3,7) using a 4:1 multiplexer.

(c) Explain a 4-bit adder cum subtraction circuit, which uses the XORs as a controlled inverter.

(d) What is the difference between a decoder and a digital multiplexer? Give four exemplary applications of a decoder.

(e) (i) Write the Mealy-FSM that recognizes the sequence 1001.

(ii) Compare Moore model and Mealy model with example.

(f) List the different types of structural styles in verilog. Write the verilog code for 4-bit full adder using gate level.

(g) How Fault is Detected in Sequential Circuit? Explain with example Path sensitization method.

(h) (i) Compare FPGA, ASIC and CPLD main features.

(ii) What do you mean by event control statements? Write a verilog code for Edge – Triggered and Level – Sensitive event control.

SECTION-C

Attempt any **two** questions from this section. **(15 x 2 = 30)**

3. Explain with example multi level minimization and optimization.
4. Design a sequential traffic-light controller for the intersection of "A" street and "B" street. Each street has traffic sensors, which detect the presence of vehicles approaching or stopped at the intersection. Draw the state graph and Verilog code for the same. (Assume all required inputs and outputs)
5. Write explanatory notes on
   a) Hazard free asynchronous circuits
   b) BDD and Ordered BDD
   c) Applications of PLD's